REMARKS

Claims 1-30 are pending. Claims 1-30 were rejected in the Office Action dated December 24, 2008. Reconsideration of all rejected claims is requested in light of the arguments and amendments presented here.

Claim Rejections Under 35 U.S.C. §103

Claims 1, 7, 11, 15, 18, 22, 29 and 30 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,829,629 to Magesacher ("Magesacher") in view of U.S. Patent No. 6,970,511 to Barnette ("Barnette").

Claim 1 recites, "a delay section comprising… a plurality of delay elements connected in series between the delay section input and the delay section output." The Office action acknowledged that these features were not shown by Magesacher, and cited Barnette (FIG. 5) instead. However, no adequate rationale is provided to combine the references and the references teach away from such a combination. The teaching away, though previously pointed out, has been ignored, and thus the rejection is improper.

The Office action (paragraph 12) indicated that one would be motivated to replace the single delay stage of Magesacher by the multiple delay stages of Barnette, "for the benefit of being able to specifically control sampling delay time, as each delay element delays the input signal by one sample delay (Barnette, column 15, lines 64-67). However, Magesacher discloses, "Each signal path has a delay stage with a delay which can be set to different values…" column 2, lines 17-18 (emphasis added). Thus, replacing the variable delay stage of Magesacher with a plurality of stages of Barnette (each apparently providing a fixed delay) would not provide a benefit in controlling delay time, but would appear to provide less flexibility in controlling delay time by limiting delay time to some integer number of sample delays. "[F]irst, second, third, fourth and fifth first-signal delay stages… each delay the single-bit input signal by one sample delay." Column 15, lines 64-67.

The Office Action (paragraph 12) further stated, "One would be motivated to make the combination as to control a decimation sequence of input signals and to provide more flexibility in delay time by allowing multiple inputs to be processed with different delays." However, this

fails to address the above argument and simply restates the rejection by indicating that more flexibility would be provided by the combination. However, there is no indication that the multiple delay stages of Barnette would provide more flexibility than the delay stage of Magesacher, which has a delay which can be set to different values. What additional flexibility is provided?

Magesacher discloses, "a decimator that converts the input value into a decimated output value..." (abstract). So control of a decimation sequence of an input signal is already provided by Magesacher, and it is not clear what additional control is referred to or why one of ordinary skill would modify the decimator of Magesacher. Barnette, FIG. 5, does not show multiple inputs to any input signal delay line processed with different delays. To the extent that Barnette shows different inputs delayed by different delays, this is achieved using different input signal delay lines 506, 511, and 515 for each input. For example, Input Signal Rin0 passes through delay stages DELAY0D0, DELAY0D1, DELAY0D2, DELAY0D3, DELAY0D4, of input signal delay line 506, but no other signal appears to pass through these delay stages. The statement in the Office action (paragraph 12), "The various delays would allow, as a result, for versatility in the different filtering functions of the different input channels," is not understood. Which input channels are referred to? Magesacher appears to show one input x_i. The inputs of Barnette FIG. 5 are provided to different input signal delay lines (as discussed above).

Furthermore, outputs from delay stages of an input signal delay line are obtained in parallel and provided to a LaGrange interpolator. "A primary first-signal delayed group DRin0a, which includes parallel outputs from the first, second, third and fourth first-signal delay stages DELAY0D0, DELAY0D1, DELAY0D2, DELAY0D3, serves as a representation of the first input signal Rin0 that is provided to the first interpolator/selector INTSEL0. The first interpolator/selector INTSEL0 employs the primary first-signal delayed group Drin0a and a signal from the oscillator TG1 to function as, in the illustrated embodiment, a merged third order LaGrange interpolator (or interpolation filter)." Column 16, lines 1-10. Thus, it is unclear how replacing delay stage 14 of Magesacher by a series of delay stages such as DELAY0D0, DELAY0D1, DELAY0D2, DELAY0D3 would provide the advantage suggested, because their outputs are provided in parallel.

Furthermore, paragraph 4 ("Response to Arguments") states, "An example [of motivation to combine the references] would be to provide an increased flexibility in processing of multiple

inputs as different delays are applied to the different inputs as shown in figure 5 of Barnette." However, figure 5 of Barnette shows input signal Rin0 provided to DELAY0D4 –DELAY0D0, input signal Rin1 provided to DELAY1D2 – DELAY1D0, and input signal Rin2 provided to DELAY2D1 – DELAY2D0. Thus, if different delays are applied to different inputs as shown in figure 5 of Barnette, each input would have a separate set of delay elements, occupying a large die area and consuming significant electrical power.

Teaching away

Replacing a single delay stage with a plurality of delay stages would generally use additional area and Barnette teaches that using significant die area is problematic. "Such hardware multipliers consume significant electrical power and require significant die area on an integrated circuit chip making such an approach problematic with a design criteria of low power and size." Column 3, lines 64-67 (emphasis added). Thus, Barnette teaches the importance of limiting area consumption and thereby teaches away from replacing a single component with multiple components in the manner proposed in the Office action.

The above teaching away by Barnette was previously presented but has been ignored. However, MPEP 707.07(f) states, "Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it" (emphasis added). MPEP 2141.03 VI states, "Prior art must be considered in its entirety, including disclosures that teach away from the claims." And MPEP 2145X.D.2 states, "References cannot be combined where reference teaches away from their combination," (emphasis added).

Independent claims 15, 29, and 30 each recite, "a delay section comprising… a plurality of delay elements." Independent claims 26, 27, and 28 each recite, "a delay section comprising… M delay elements," and "M>1." As discussed with respect to claim 1, these features are not taught or suggested by the cited references. Therefore, claims 15, 26, 27, 28, and 29 are submitted to be allowable. Furthermore, claim 30 is directed to "a computer program product… stored on a computer storage media… comprising: computer code that, when executed by a processor, programs a device to create a programmed device, wherein the programmed device

comprises..." No prior art features were identified as corresponding to these features of claim 30 (which was rejected on the same basis as claim 1) and it does not appear that the devices shown by Magesacher or Barnette are such programmed devices.

All dependent claims depend from one of the independent claims above and are therefore submitted to be allowable at least for depending from an allowable base claim. Furthermore, the dependent claims recite additional features that have not been shown in the cited references.

Claims 13, 14, 24, and 25 were rejected under 35 U.S.C. §103(a) as being unpatentable over Magesacher in view of Barnette as applied to claims 1 and 15 above, and further in view of U.S. Patent No. 4,999,798 to McCaslin et al. ("McCaslin"). "). However, McCaslin does not cure the defects in the rejections of claims 1 and 15 discussed above and thus these claims are allowable at least for depending from allowable base claims.

Claims 2-5, 8-10, 12, 16, 19, 20, 21, and 23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Magesacher in view of Barnette and further in view of Applicant admitted prior art ("AAPA"). However, AAPA does not cure the defects in the rejections of claims 1 and 15 discussed above and thus these claims are allowable at least for depending from allowable base claims. Furthermore, these claims recite additional features that have not been identified in the references.

For example, claim 5 recites, "the plurality of delay elements comprises at least M delay elements, each delay element of the plurality of delay elements delaying each of the M channel's data and providing an output that is specific to an individual channel of the M channels." The Office action cited input signal delay lines 506, 511, and 516 of Barnette, FIG. 5 as showing these features. However, none of these signal delay lines (or their delay stages) delays each of the input signals, because the signal delay lines are each dedicated to a specific input signal. "The first section 505 includes a first input signal delay line 506 that receives the first input signal Rin0... The second section 510 includes a second input signal delay line 511 that receives the second input signal Rin1...The third section 515 includes a third input signal delay line 515

that receives the third input signal Rin2..." column 15, lines 52-61. Because these features have not been shown, claim 5 is submitted to be additionally allowable.

Claims 6, 17, and 26-28 were rejected under 35 U.S.C. §103(a) as being unpatentable over Magesacher in view of Barnette and AAPA, and further in view of U.S. Patent No. 4,686,655 to Hyatt ("Hyatt").

The Office Action acknowledged that Magesacher, Barnette, and AAPA failed to disclose "a multiplexer that multiplexes M channels and provides a multiplexed signal to the integrator" of claim 6. Analog multiplexer 220 of Hayatt was cited. "Amplified and filtered signals 215 may be received from a plurality of channels... and may be multiplexed with analog multiplexer 220 to be sequentially converted with analog-to-digital converter (ADC) 222 for input to a computer 223 and for storage in memory 224." Column 43, lines 28-34. The cited motivation for combining the analog multiplexer of Hayatt with Magesacher etc, "for the benefit of creating more flexibility" is not clear. What additional flexibility is obtained by replacing the digital input value x_i of Magesacher (or input signals Rin0, Rin1, and Rin2 of Barnette) with a multiplexed analog signal obtained from M channels? And how would the analog signal produced by analog multiplexer 220 be used in such an apparatus?

Claims 26-28 each recite, "a delay section comprising:... M delay elements" in combination with other elements. However, such combinations have not been shown in the cited references as discussed with respect to claim 1. Claims 26-28 each further recite, "a multiplexer." However, because no adequate rationale has been provided for combining the multiplexer of Hayatt with the integrator of Magesacher, obviousness has not been shown.

CONCLUSION

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. However, if the Examiner has any further matters that need to be resolved, a telephone call to the undersigned at 510-663-1100 would be appreciated.

Respectfully submitted,
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